

CLAIMS

What is claimed is:

- Sub
A1
- 1 1. A circuit, comprising:
- 2 a first control register to be loadable after the circuit is reset;
- 3 a first plurality of control registers to be loadable during an initialization
- 4 process after the circuit is reset and to be unloadable until the circuit is reset again;
- 5 and
- 6 a first switch unit coupled to the first control register and the first plurality of
- 7 control registers, wherein the first switch unit to output data stored by one control
- 8 register of the first plurality of control registers as a function of the data loaded in the
- 9 first control register.
- 1 2. The circuit of claim 1, wherein the first switch unit comprises a multiplexer
- 2 having input ports coupled to receive output from the first plurality of control registers
- 3 and having a control port coupled to receive output from the first control register.
- 1 3. The circuit of claim 1, wherein the first control register is loadable through
- 2 software control after the circuit is reset.
- 1 4. The circuit of claim 3, wherein the software control to cause the first register
- 2 to be loaded with different data in response to a change in the circuit's operational
- 3 mode.
- 1 5. The circuit of claim 1, wherein the circuit is a memory controller.

1 6. The circuit of claim 1, wherein the first plurality of control registers to be
2 loaded by a basic input output system (BIOS) during an initialization process after
3 the circuit is reset.

1 7. The circuit of claim 6, wherein the first plurality of control registers to be
2 locked by the BIOS during the initialization process after the circuit is reset.

1 8. The circuit of claim 7, wherein the first plurality of control registers each
2 include a lock bit to be set by the BIOS to lock the first plurality of control registers
3 during the initialization process after the circuit is reset.

1 9. The circuit of claim 1, further comprising:
2 a second control register to be loadable after the circuit is reset;
3 a second plurality of control registers to be loadable during the initialization
4 process and to be unloadable until the circuit is reset again; and
5 a second switch unit coupled to the second control register and the second
6 plurality of control registers, wherein the second switch unit to output data stored by
7 one control register of the second plurality of control registers as a function of the
8 data loaded in the second control register.

*2 circuits with reference
1 5 of
figure 1*

1 10. A circuit, comprising:
2 means for storing first data and second data, the second data including a
3 plurality of portions, wherein, after the circuit is reset and initialized the first data is
4 changeable and the second data is not changeable; and
5 means for selecting one portion of the plurality of portions in response to the
6 first data, wherein the selected portion to be provided to another unit of the circuit.

1 11. The circuit of claim 10, wherein the means for selecting comprises a
2 multiplexer having input ports coupled to receive the second data and having a
3 control port coupled to receive the first data.

1 12. The circuit of claim 10, wherein after the circuit is reset and initialized, the
2 means for storing further for changing the first data in response to software control.

1 13. The circuit of claim 12, wherein the software control causes the first data to
2 be changed in response to a change in the circuit's operational mode.

1 14. The circuit of claim 13, wherein the circuit's operational mode is user-
2 selectable.

1 15. The circuit of claim 10, wherein the means for storing is loadable with the first
2 data by a basic input output system (BIOS) during the initialization process.

1 16. The circuit of claim 15, wherein the means for storing is locked by the BIOS to
2 prevent changes to the first data after the initialization process is performed, the
3 second data remaining changeable.

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1 17. A method, comprising:
2 storing first data and second data in a circuit, the second data including a
3 plurality of portions, wherein, after the circuit is reset and initialized, the first data is
4 changeable and the second data is not changeable; and
5 selecting one portion of the plurality of portions in response to the first data,
6 wherein the selected portion to be provided to another unit of the circuit.

3 selecting another locked control register of the plurality of protected control
4 registers.

1 25. An circuit, comprising:
2 a plurality of control registers;
3 means for loading the plurality of control registers, the plurality of control
4 registers including a plurality of protected registers and unprotected registers;
5 means for locking the plurality of protected control registers;
6 means for selecting a locked control register of the plurality of control
7 registers; and
8 means for outputting data stored by the selected locked control register.

1 26. The circuit of claim 25, wherein the means for selecting selects the locked
2 control register as a function of data stored in an unprotected control register of the
3 plurality of control registers.

1 27. The circuit of claim 25, further comprising:
2 means for deselecting the locked control register; and
3 means for selecting another locked control register of the plurality of protected
4 control registers.

1 28. A system, comprising:
2 a processor;
3 a memory; and
4 a memory controller coupled to the processor and the memory, the memory
5 controller comprising:

6 a first control register to be loadable after the memory controller is
7 reset;

8 a first plurality of control registers to be loadable during an initialization
9 process after the memory controller is reset and to be unloadable after initialization
10 until the circuit is reset again; and

11 a first switch unit coupled to the first control register and the first
12 plurality of control registers, wherein the first switch unit to output data stored by one
13 control register of the first plurality of control registers as a function of the data
14 loaded in the first control register.

1 29. The system of claim 28, wherein the first switch unit comprises a multiplexer
2 having input ports coupled to receive output from the first plurality of control registers
3 and having a control port coupled to receive output from the first control register.

1 30. The system of claim 28, wherein the first control register is loadable in
2 response to software control after the circuit is initialized.